



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,652	11/12/2003	Kang-Deog Suh	4591-344	8964
20575	7590	08/23/2005	EXAMINER	
MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204			NGUYEN, TAN	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/712,652	SUH ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 August 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-10 is/are allowed.
- 6) ☒ Claim(s) 1, 4 and 11 is/are rejected.
- 7) ☒ Claim(s) 2, 3 and 12-16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date: _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date: _____  | 6) <input type="checkbox"/> Other: _____                                    |

1. The following action is in response to the amendment submitted by Applicants on August 10, 2005.
2. The drawing correction submitted by Applicants on August 10, 2005 has been received.
3. Claims 1-16 are pending.
4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 4 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Endoh et al. (U.S. Patent No. 5,469,444).

Endoh et al. disclosed in Figure 1 a EEPROM device [10] having a memory cell array [12] (column 4, line 2) coupled to a word line controller [14] (column 9-13), which is coupled to a verify voltage generator [24] (column 4, line 39). In Figure 7, Endoh et al. disclosed the detail of the word line controller [14] includes five voltage generating circuits connected to word line [WLj]: a high voltage supply circuit [102] for write operation, a midlevel voltage supply circuit [104] for nonselected word line in write operation, a first verify-voltage supply circuit [106], a second verify-voltage supply circuit [108] for write verify operation, and an erase/read control circuit [110] for erase operation (column 7, lines 61-65 and column 7, line 68 to column 8, line 24). In Figure 8, Endoh et al. disclosed a voltage generation circuitry for providing the circuit [106,108] with the two verify voltages [Vver1, Vver2] that includes a voltage divider [126] to vary

Art Unit: 2827

the verify voltages [Vver1, Vver2] (column 9, lines 18-20, lines 49-51). Accordingly, the voltage generation circuitry [120] would be considered as the claimed program verification voltage generator since it variably generates program verification voltage [Vver1, Vver2], and the first and second verify-voltage supply circuits [106, 106] of the word line controller [14] would be considered as the claimed word line level selector since they transfer the verify-voltages [Vver1, Vver2] to the word lines.

Regarding claim 4, Endoh et al. disclosed the word line controller [14] includes five voltage generating circuits connected to word line [WLj]: a high voltage supply circuit [102] for write operation, a midlevel voltage supply circuit [104] for nonselected word line in write operation, a first verify-voltage supply circuit [106], a second verify-voltage supply circuit [108] for write verify operation, and an erase/read control circuit [110] for erase operation (column 7, lines 61-65 and column 7, line 68 to column 8, line 24).

Regarding claim 11, in Figure 8, Endoh et al, further disclosed the voltage input terminals [122, 124] to which the write-verify control signals [W-VERIFY1, W-VERIFY2] are supplied (column 9, lines 31-32).

6. Claims 2-3 and 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 5-10 are allowed.

8. The following is an examiner's statement of reasons for allowance:

The prior art failed to show or suggest the structure of the program verification voltage generator in claims 2-3, the limitation of the programming unit loop cycle wherein the program verification voltages are changed between two or more program unit loop cycles as in claims 5-10, or the detail of the second input structure as in claims 12-15

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Noguchi, Kobayashi et al., Tomoeda, Lee et al. and Roohpavar are cited to show memory devices having program verify circuit coupled to the row decoder.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

Art Unit: 2827

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen  
Primary Examiner  
Art Unit 2827  
August 18, 2005